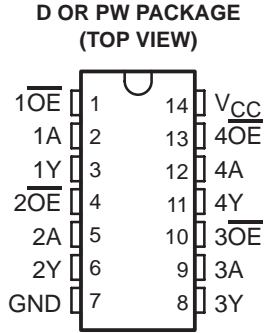


SN74AHCT125-Q1 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCLS508A – JUNE 2003 – REVISED FEBRUARY 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Inputs Are TTL-Voltage Compatible



description/ordering information

The SN74AHCT125 is a quadruple bus buffer gate featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high. When \overline{OE} is low, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION†

| T_A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| –40°C to 125°C | SOIC – D | Tape and reel | SN74AHCT125QDRQ1 | AHCT125Q |
| | TSSOP – PW | Tape and reel | SN74AHCT125QPWRQ1 | HB125Q |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

FUNCTION TABLE (each buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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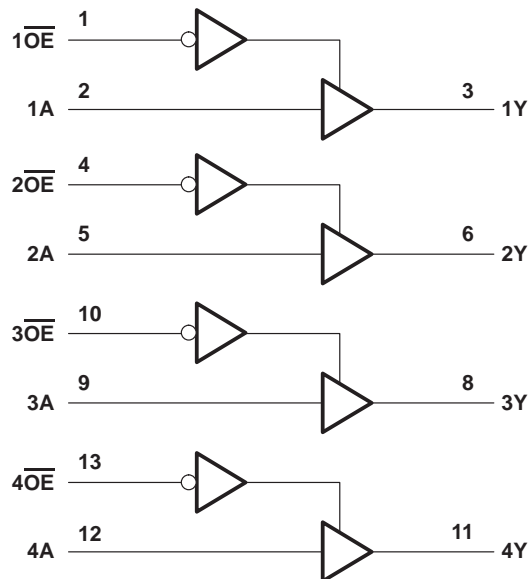
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SN74AHCT125-Q1

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the D and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|-----|-----------------|------|
| V _{CC} | Supply voltage | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | V |
| V _I | Input voltage | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -8 | mA |
| I _{OL} | Low-level output current | | 8 | mA |
| Δt/Δv | Input transition rise or fall rate | | 20 | ns/V |
| T _A | Operating free-air temperature | -40 | 125 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-------------------------------|---|-----------------|-----------------------|-----|-------|------|-----|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | I _{OH} = -8 mA | | | | 3.94 | | 3.8 | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | | 0.1 | 0.1 | | V |
| | I _{OL} = 8 mA | | | | 0.36 | 0.44 | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | ±1 | | μA |
| I _{OZ} | V _O = V _{CC} or GND | 5.5 V | | | ±0.25 | ±2.5 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 2 | 20 | | μA |
| ΔI _{CC} [†] | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 1.35 | 1.5 | | mA |
| C _i | V _I = V _{CC} or GND | 5 V | | 4 | 10 | 10 | | pF |
| C _o | V _O = V _{CC} or GND | 5 V | | 15 | | | | pF |

[†] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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QUADRUPLE BUS BUFFER GATE

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|-----|-----|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t_{PLH} | A | Y | $C_L = 15\text{ pF}$ | 3.8 | 5.5 | 1 | 6.5 | ns | |
| t_{PHL} | | | | 3.8 | 5.5 | 1 | 6.5 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 15\text{ pF}$ | 3.6 | 5.1 | 1 | 6 | ns | |
| t_{PZL} | | | | 3.6 | 5.1 | 1 | 6 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 15\text{ pF}$ | 4.6 | 6.8 | 1 | 8 | ns | |
| t_{PLZ} | | | | 4.6 | 6.8 | 1 | 8 | | |
| t_{PLH} | A | Y | $C_L = 50\text{ pF}$ | 5.3 | 7.5 | 1 | 8.5 | ns | |
| t_{PHL} | | | | 5.3 | 7.5 | 1 | 8.5 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 50\text{ pF}$ | 5.1 | 7.1 | 1 | 8 | ns | |
| t_{PZL} | | | | 5.1 | 7.1 | 1 | 8 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 50\text{ pF}$ | 6.1 | 8.8 | 1 | 10 | ns | |
| t_{PLZ} | | | | 6.1 | 8.8 | 1 | 10 | | |
| $t_{sk(o)}$ | | | $C_L = 50\text{ pF}$ | | | 1 | 1 | ns | |

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | | MIN | MAX | UNIT |
|-------------|--|-----|------|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | 4.4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

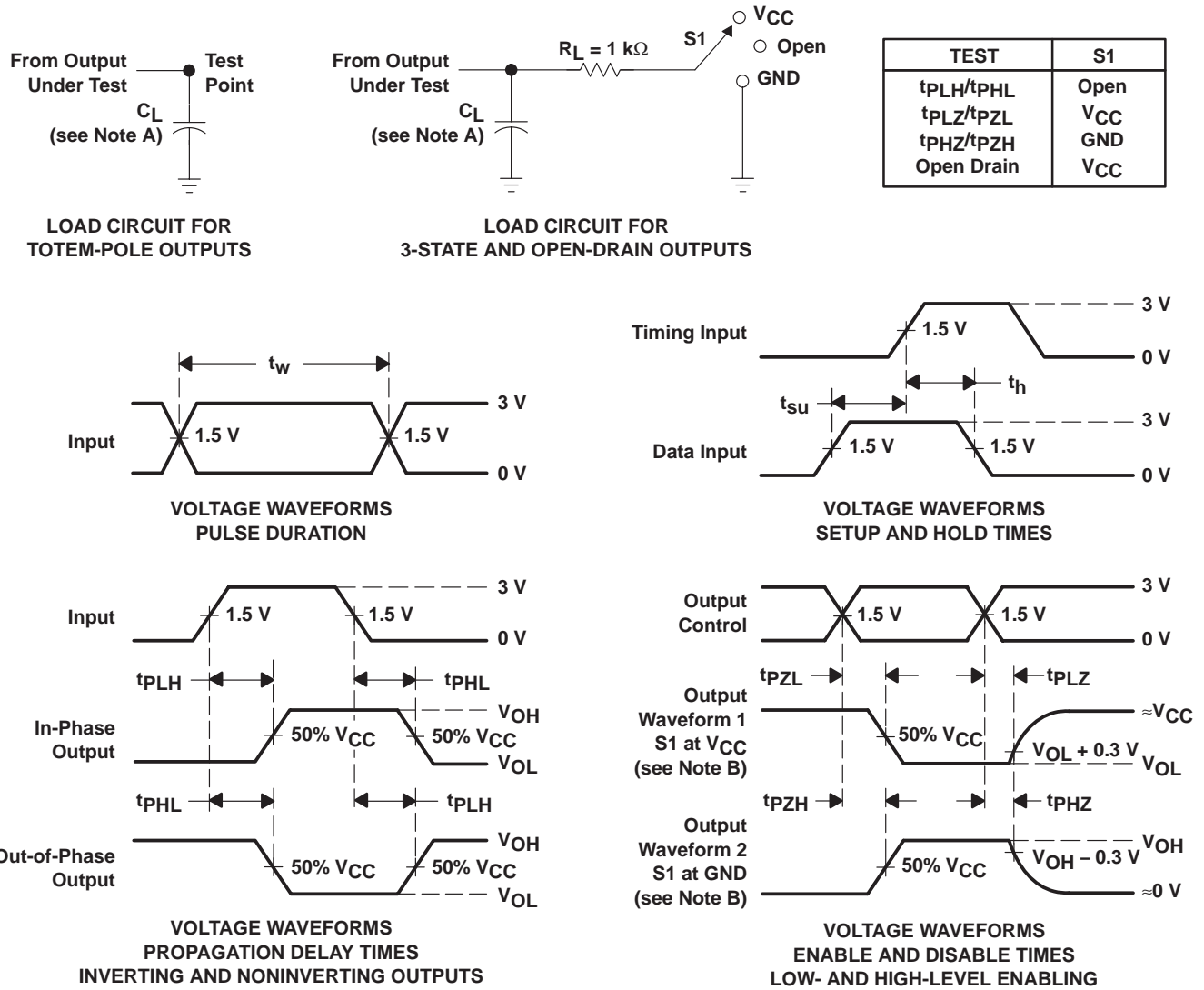
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------|-------------------------------|-----------------------------|-------|
| C_{pd} | Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 14 pF |



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| CAHCT125QPWRG4Q1 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHCT125QDRG4Q1 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHCT125QDRQ1 | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74AHCT125QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Catalog: [SN74AHCT125](#)
- Enhanced Product: [SN74AHCT125-EP](#)
- Military: [SN54AHCT125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

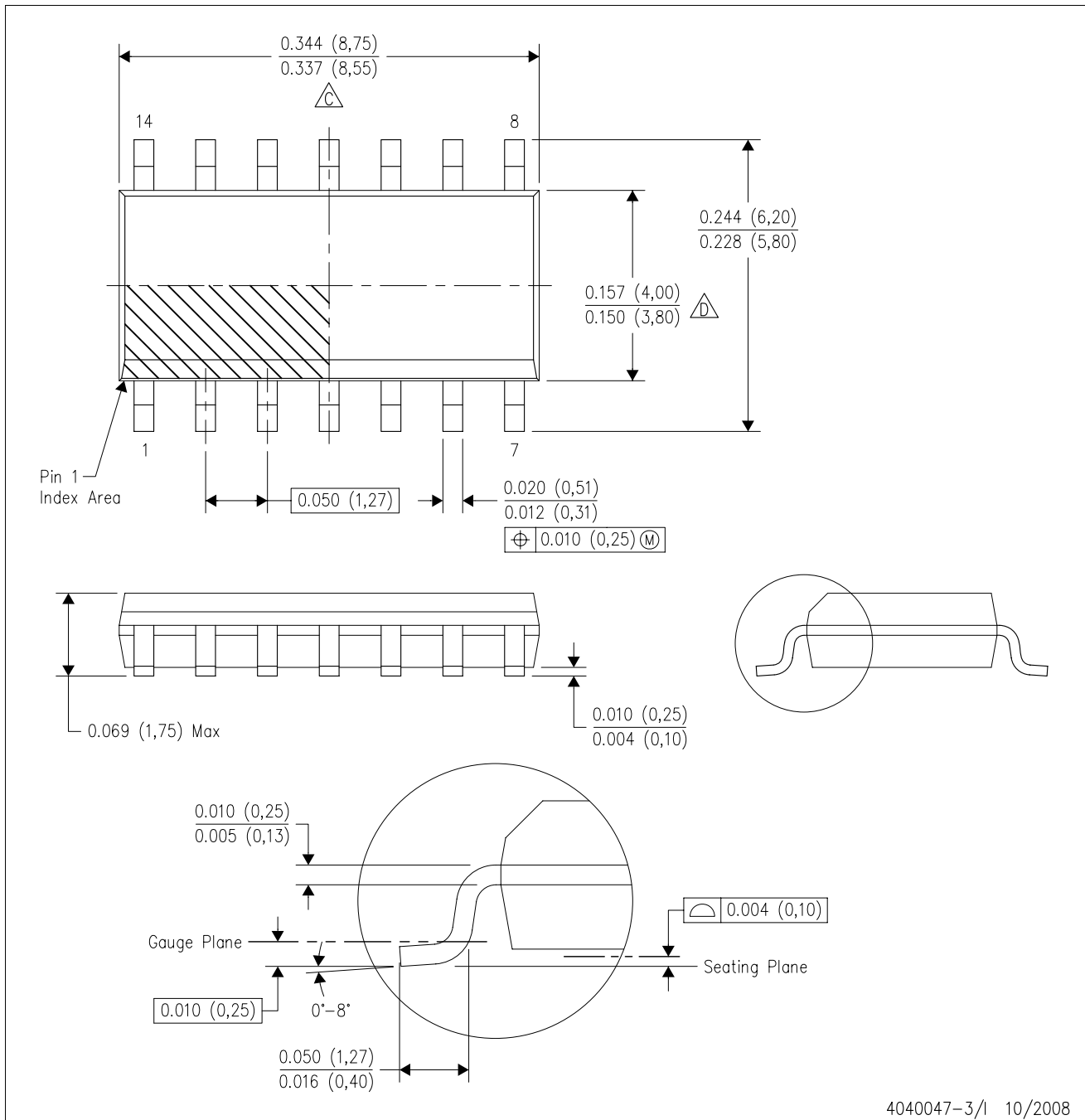


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- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

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